Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method of operating a processor to repeatedly execute an instruction, comprising:

determining at run time how many times a single instruction is to be repeated;

loading at run time an existing general purpose register with a count value indicative of the number of times a single instruction is to be executed;

fetching and executing a REPEAT instruction, the REPEAT instruction indicating the single instruction to be repeatedly re-executed;

fetching the single instruction; and

repeatedly executing the single instruction for a consecutive number of times as indicated by the count value without refetching the single instruction and without adding a NOP (no operation) instruction;

adjusting the count value in the register each time the single instruction is executed during an execution phase.

2. (Currently Amended) A method of operating a processor to repeatedly execute an instruction comprising:

fetching a REPEAT instruction;

executing a REPEAT instruction, wherein execution of the REPEAT instruction determines and stores at run time in [[a]] an existing general purpose register a count value indicative of the number of times a single instruction is to be executed;

fetching the single instruction; and

repeatedly executing the single instruction consecutively for as many times as indicated by the count value without re-fetching the single instruction and without fetching any other instruction and without adding a NOP (no operation) instruction;

decrementing the count value in the register each time the single instruction is executed; and

incrementing a program counter once the count value in the register is one of less than zero and equal to zero, thereby providing an effective data rate of one transfer every clock cycle;

wherein decrementing the count value in the register does not start until ~~repeatedly~~ an execution phase for executing the single instruction begins .

3. (Currently Amended) A method of operating a processor to repeatedly execute an instruction comprising:

determining at run time a count value indicative of how many times a single instruction is to be repeated;

loading at run time a general purpose register with the count value indicative of the number of times a single instruction is to be executed;

fetching and executing a REPEAT instruction indicating the single instruction that is to be repeatedly executed;

incrementing a program counter;

fetching the single instruction;

repeatedly executing the single instruction for as many times as indicated by the count value stored in the register without refetching the single instruction and without fetching any other instruction and without adding a NOP (no operation) instruction;

decrementing the count value stored in the register each time the an execution phase for the single instruction is executed; and

stalling the program counter until the count value in the register is one of less than zero and equal to zero, thereby providing an effective data rate of one transfer every clock cycle;

wherein decrementing the count value in the register does not start until repeatedly executing the single instruction begins.

4. (Original) A method of operating a processor according to claim 3, wherein said count value is stored in said count register before execution of said REPEAT instruction.

Claims 5-6 (Cancelled)

7. (Previously Presented) A method according to claim 3, wherein method further comprises:

determining whether said count value is less than or equal to zero.

8. (Currently Amended) A processor for repeatedly executing a single instruction, said processor comprising:

means for determining at run time a count value indicative of how many times a single instruction is to be repeated;

means for loading at run time a general purpose register with [[a]]the count value indicative of the number of times the single instruction is to be executed;

means for fetching a REPEAT instruction, the REPEAT instruction indicating the single instruction to be repeatedly executed;

means for executing the REPEAT instruction indicating the single instruction to be repeatedly executed;

means for fetching the single instruction; [[and]]

means for repeatedly executing the single instruction a consecutive number of times as indicated by the count value without refetching the single instruction and without adding a NOP (no operation) instruction; and

means for adjusting the count value in the register each time when an execution phase for the single instruction is executed

wherein the means for adjusting the count value only operates when the means for repeatedly executing the single instruction is executing the single instruction.

9. (Currently Amended) A processor for repeatedly executing an instruction, comprising:

means for determining at run time how many times a single instruction is to be repeated;

means for fetching a REPEAT instruction;

means for executing a REPEAT instruction, wherein execution of the REPEAT instruction at run time stores in a general purpose register a count value indicative of the number of times a single instruction is to be executed;

means for fetching the single instruction;

means for repeatedly executing the single instruction for as many times as indicated by the count value without re-fetching the single instruction and without fetching any other instruction and without adding a NOP (no operation) instruction;

means for decrementing the count value in the register each time an execution phase for the single instruction is executed; and

means for incrementing a program counter once the count value in the register is less than zero, thereby providing an effective data rate of one transfer every clock cycle;

wherein the means for decrementing only operates while the means for repeatedly executing the single instruction is executing the single instruction.

10. (Currently Amended) A processor for repeatedly executing an instruction, comprising:

means for determining at run time how many times a single instruction is to be repeated;

means for loading a general purpose register at run time with a count value indicative of the number of times a single instruction is to be executed;

means for fetching a REPEAT instruction indicating the single instruction that is to be repeatedly executed;

means for executing the REPEAT instruction indicating the single instruction that is to be repeatedly executed without adding a NOP (no operation) instruction;

means for incrementing a program counter;

means for fetching the single instruction; and

means for repeatedly executing the single instruction for a consecutive number of times as indicated by a count value stored in a count register without refetching the single instruction and without fetching any other instruction;

means for decrementing the count value stored in the register each time the single instruction is executed; and

means for ~~means for~~ incrementing a program counter once the count value in the register is equal to zero, thereby providing an effective data rate of one transfer every clock cycle

wherein the means for decrementing only operates while the means for repeatedly executing the single instruction is operating in an execution phase executing the single instruction.

11. (Original) A processor according to claim 10, wherein said count value is stored in said count register before execution of said REPEAT instruction.

Claims 12 – 13 (Cancelled)

14. (Previously Presented) A processor according to claim 10, wherein the processor further comprises:

means for determining whether said count value is less than or equal to zero.

15. (Currently Amended) A processor for repeatedly executing one or more processor instructions, said processor comprising:

a memory address register associated with a main memory;

a memory data register associated with the main memory;

a memory control for generating memory control signals;

a program counter for storing a memory address location of the main memory where an instruction is to be fetched;

an instruction register for storing an instruction that is to be executed;

at least one general purpose register for storing a count;

decode and execute control logic for decoding and executing an instruction stored in the instruction register; and

a state machine for controlling the fetching and repeated execution of a single instruction, the state machine configured to repeatedly execute the single instruction by signaling the instruction register to hold the same instruction and not fetch the next instruction and to decrement the count stored in the general purpose register each time the single instruction is executed, and to signal the program counter not to increment until the count stored in the general purpose register is below a threshold value, thereby providing an effective data rate of one transfer every clock cycle;

wherein ~~the state machine only decrements the count stored in the general purpose register while the single instruction is executed~~ a next instruction following the single instruction is not fetched until after the repeated execution of the single instruction has completed .

16. (Cancelled)

17. (Original) A processor according to claim 15, wherein said general purpose register includes a first register for storing a count value indicative of the number of times the single instruction is to be repeatedly executed.

Claims 18-22 (Cancelled)

23. (Previously Presented) The processor of claim 15, wherein the state machine is configured to increment the program counter once the count value is equal to zero.

24. (Previously Presented) The processor of claim 15, further comprising the state machine configured to increment the program counter once the count value is less than zero.

25. (Cancelled)

26. (Previously Presented) The processor for repeatedly executing a single instruction of claim 8, further comprising means for incrementing a program counter once the count value is equal to zero.

27. (Previously Presented) The processor for repeatedly executing a single instruction of claim 8, further comprising means for incrementing a program counter once the count value is less than zero.

28. (Previously Presented) The processor for repeatedly executing a single instruction of claim 8, wherein a program counter remains unchanged as the single instruction is repeatedly executed.

29. (Previously Presented) The method of operating a processor to repeatedly execute an instruction of claim 2, wherein the program counter remains unchanged as the single instruction is repeatedly executed.

30. (Previously Presented) The method of operating a processor to repeatedly execute an instruction of claim 2, wherein the program counter is effectively stalled on the single instruction.

31. (Previously Presented) The method of operating a processor to repeatedly execute an instruction of claim 3, wherein the program counter remains unchanged as the single instruction is repeatedly executed.

32. (Previously Presented) The method of operating a processor to repeatedly execute an instruction of claim 3, wherein the program counter is effectively stalled on the single instruction until the single instruction executes the number of times indicated by the count value.

33. (Canceled)

34. (New): A method of operating a processor to repeatedly execute an instruction in a pre-emptive multi-tasking environment, comprising:

determining at run time how many times a single instruction is to be repeated;

loading at run time an existing general purpose register with a count value indicative of the number of times a single instruction is to be executed;

fetching and executing a REPEAT instruction, the REPEAT instruction indicating the single instruction to be repeatedly re-executed;

fetching the single instruction;

repeatedly executing the single instruction for a consecutive number of times as indicated by the count value without refetching the single instruction and without adding a NOP (no operation) instruction;

adjusting the count value in the register each time the single instruction is executed;

suspending the repeatedly executing the single instruction step while a second context executes; and

resuming the repeatedly executing the single instruction after the second context executes;

wherein contents of an instruction buffer containing the single instruction are locked and preserved while the second context executes.

35. (New): A method according to claim 34, wherein said count value is stored before execution of said REPEAT instruction.

36. (New): A method according to claim 34, wherein said REPEAT instruction includes the count value that is stored in said count register, wherein execution of the REPEAT instruction stores the count value in said count register.

37. (New) A method according to claim 34, further comprising:

incrementing the program counter after the one or more associated instructions have been executed for as many times as indicated by the count value.

38. (New): A method according to claim 34, wherein the adjusting the count value further comprises:

decrementing said count value stored in said register each time said one or more associated instructions are executed; and

determining whether said count value is less than or equal to zero.

39. (New): A processor configured to repeatedly execute an instruction in a pre-emptive multi-tasking environment, comprising:

means for determining at run time how many times a single instruction is to be repeated;

means for loading at run time an existing general purpose register with a count value indicative of the number of times a single instruction is to be executed;

means for fetching and executing a REPEAT instruction, the REPEAT instruction indicating the single instruction to be repeatedly re-executed;

means for fetching the single instruction;

means for repeatedly executing the single instruction for a consecutive number of times as indicated by the count value without refetching the single instruction and without adding a NOP (no operation) instruction;

means for adjusting the count value in the register each time the single instruction is executed;

means for suspending the repeatedly executing the single instruction step while a second context executes; and

means for resuming the repeatedly executing the single instruction after the second context executes;

wherein contents of an instruction buffer containing the single instruction are locked and preserved while the second context executes.

40. (New): A processor according to claim 39, wherein said count value is stored before execution of said REPEAT instruction.

41. (New): A processor according to claim 39, wherein said REPEAT instruction includes the count value that is stored in said register, wherein the means for fetching and executing the REPEAT instruction stores the count value in said register.

42. (New) A processor according to claim 39, further comprising:

means for incrementing the program counter after the one or more associated instructions have been executed for as many times as indicated by the count value.

43. (New): A processor according to claim 39, wherein the means for adjusting the count value further comprises:

means for decrementing said count value stored in said register each time said one or more associated instructions are executed; and

means for determining whether said count value is less than or equal to zero.

44. (New): A processor for repeatedly executing one or more processor instructions, said processor comprising:

a memory address register associated with a main memory;

a memory data register associated with the main memory;

a memory control for generating memory control signals;

a program counter for storing a memory address location of the main memory where an instruction is to be fetched;

an instruction register for storing an instruction that is to be executed;

at least one general purpose register;

decode and execute control logic for decoding and executing an instruction stored in the instruction register; and

a state machine for controlling the fetching and repeated execution of one or more associated instructions.

wherein the processor is operating in a pre-emptive multi-tasking environment, further comprising the processor configured to suspend executing the instruction in the instruction register while a second context execute, and the processor is configured to resume executing the instruction in the instruction register after the second context executes;

wherein contents of an instruction buffer are locked and preserved while the second context executes.

45. (New) A processor according to claim 44, wherein said general purpose register includes a first register for storing a count value indicative of the number of times the one or more associated instructions are to be repeatedly executed.

46. (New) A processor according to claim 45, wherein said state machine generates signals for decrementing the count value stored in the first register.

47. (New): A processor according to claim 44, wherein said state machine generates a signal for executing an instruction stored in said instruction register.

48. (New) A processor according to claim 44, wherein said state machine generate a signal for incrementing said program counter.